## REMARKS

This paper is responsive to the Office Action dated September 6, 2005. Claims 1-28 were examined, all of which have been rejected.

In the present Office Action: claims 1, 9 and 10 were objected to; and claims 1-28 were rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,550,050 (hereinafter "Hosono"). Applicants note that Hosono issued on April 15, 2003, prior to the filing date (i.e., September 8, 2003) of Applicants' application.

Applicants have amended claims 4, 9, 10, 14, 16-18 and 26 for clarification and/or to address valid issues raised by the present Office Action. Applicants respectfully submit that the objections to claims 9 and 10 are now moot. With respect to the objection to claim 1, as is further discussed below, in view of Applicants' specification, Applicants respectfully submit that the term "feature sizes" is clear.

As is set forth in Applicants' independent claims 1, 11, 17 and 23, in one form or another, information, associated with circuit devices directly connected to an input of a circuit, is extracted from a circuit description of the circuit. The extracted information includes information related to device connectivity and feature sizes. The feature sizes are aggregated to obtain an aggregate feature size and a total capacitance of the input is determined based, at least in part, on the aggregate feature size. With reference to, for example, Applicants' paragraph 1022 (at pages 5-6), the information related to feature sizes may include a length, width and depth of various device features, a location and size of conductive paths, and any other information that might be useful to determine the capacitive effect of a feature on an input or output to which the feature is connected. For example, with reference to Applicants' paragraph 1024 (pages 6-7), assuming gates (having a width of six microns each) of four N-type metal oxide semiconductor (NMOS) transistors and gates (having a width of three microns each) of four P-type metal oxide semiconductors (PMOS) are directly connected to a circuit input being analyzed, an aggregate gate width directly connected to the input being analyzed is thirty-six microns. That is, the NMOS transistors have a feature size of six microns and the PMOS transistors each have a feature size of three microns, with an aggregate feature size being equal to thirty-six microns in this example.

With reference to Applicants' specification (see, for example paragraph 1027 at page 7), in addition to aggregating different feature types, multiple dimensions of a particular feature may be used to generate an aggregate feature size. For example, length and width may be used to generate an aggregate feature size based on area. As another example, length, width and height may be used to generate an aggregate feature size based on volume. Thus, Applicants respectfully submit that the term "feature sizes" is clear in view of Applicants' specification, and, as such, the objection to claim 1 should be withdrawn.

Moreover, Applicants submit that the rejection of claims 1, 11, 17 and 23, as being anticipated by Hosono, is in error and should be withdrawn. More specifically, Applicants submit that none of the Hosono cited passages teach or suggest utilization of feature sizes of circuit devices connected directly to an input of a circuit. Additionally, Applicants submit that Hosono does not teach or suggest aggregating feature sizes of circuit devices connected to an input of a circuit to obtain an aggregate feature size to determine a total capacitance of the input, based, at least in part, on the aggregate feature size. With specific reference to Hosono col.1, lines 28-38, the cited passage merely discloses summing input load capacitances of all next-stage circuit cells connected to an output to determine a load capacitance of the output. A warning is then issued if the capacitance exceeds a value which would cause unacceptable waveform rounding and gate delay times. Applicants further submit that the cited passage provides no disclosure on how a capacitance is determined. With respect to Hosono col. 3, lines 24-59, Applicants submit that the cited passage merely discloses a series of steps which include: a longest wiring load calculating first step, a wiring load estimating second step and a determining step. The determining step essentially compares a first load found in the first step and a second load found in the second step to determine whether waveform rounding is acceptable, i.e., whether the second load is less than the first load. Additionally, Applicants note that Hosono discloses calculating a capacitance (CEL) by first converting a longest wiring resistance (RWL) into a capacitance based on a delay time determined by a derived $\pi$-type wiring load model (see col. 7, lines 25-62).

In summary, Applicants submit that Hosono does not teach, or suggest, determining a load capacitance of an input based, at least in part, on an aggregate feature size of circuit devices connected to an input. For at least the above reasons, Applicants respectfully submit

independent claims 1, 11, 17 and 23 are allowable over Hosono. Furthermore, Applicants submit that dependent claims 2-10, 12-16, 18-22 and 24-28 are also allowable for at least the reason that they depend upon an allowable claim.

In summary, claims 1-28 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone; the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

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